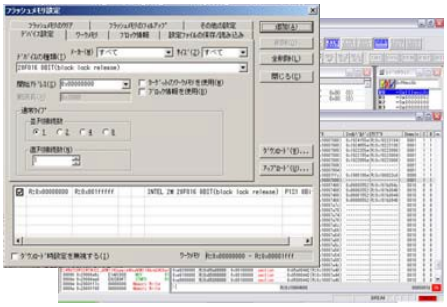
Sohwa & Sophia Technologies

Product Brief

WATCHPOINT Debugger for EJ-SCT Xtensa / Xtensa Multi Core



This software is used in combination with our JTAG emulator “EJSCT”.

- Small size (70mm × 108mm × 17mm)
- Powered by USB bus when using in connection with PC

Features

- Supports Tensilica licensed Xtensa LX
- Debugs multiple Tensilica Xtensa core CPUs at one time. *1
- Supports ICE interface specified by Tensilica
- Supports Tensilica’s Diamond Standard Processors *2
- Supports TIE, FLIX instruction
- View and modify internal peripheral registers
- 4 hardware breakpoints
  (Instruction address: 2 poitns, Data address: 2 points)
- Unlimited software breakpoints
- Supports the semi-hosting capability
- Supports C/C++ (OS: Windows Vista/7)
- USB2.0 host interfaces for high-speed communication with host computer
- One common hardware unit supports other CPU series by purchasing software license additionally
- Download capability to flash memory
- Writes to on-board and CPU internal flash memory
- Useable as a stand-alone writer.（operate by AC adaptor)
- One-touch automatic script execution via the PLAY button on the unit
- The external terminal setup for executing a script by signal input and detecting the end state of a script externally
- Perfect for use in auto-verification of the target on mass production or for updating new versions

Specifications

Target CPU *2 tensilica	T1020, T1030, T1040, T1050, Xtensa LX, Xtensa6, Xtensa7, Xtensa LX2, LX3, LX4 Diamond Standard Processors (Supports the ASIC with the on-chip debugging interface) 106Micro, 108Mini, 212GP, 232L, 570T, 545CK, 330HiFi, 388VDO
Target Vcc	Vcc= +1.8 V to 3.6 V
Memory and I/O	Entire space is available to user
Interrupts	Both internal and external interrupts are available to user
Breakpoints and Break Options	Execution address break options: ・Hardware breakpoints: Instruction:2 points, Data: 2 points* Execution instruction address and memory access can be specified. * The number of hardware breakpoints (BP) will be specified when configuring the CPU. * Upon configuring the CPU, 2 instruction execution addresses and 2 data access addresses must be specified. ・Unlimited software breakpoints Other break options: ・Forced break from the debugger
Flash Memory	Download to target external Flash memory ・Possible to write to not-supported flash memory when users make a custom program ・Stand-alone writer capability Without a command from the computer, users can download to flash memory by recording flash memory writing script into the attached MicroSD. (Two different operation scripts can be recorded)
Trace feature	Regarding the trace feature, WATCHPOINT debugger can support the XtensaLX feature that installs the trace feature. Please contact us about more details about the trace feature.

*1 Please specify WATCHPOINT (WP DBG for EJS Xtensa MC) for debugging Multi Processor Core.
Max 10 CPUs can be debugged at the same time. But the CPU internal configuration or PC environment may have an effect on the number of CPUs being debugged.
*2 The EJ-SCT Debugger for Xtensa LX supports Xtensa6 and Diamond Standard Processors, but does not support the MMU capability of these CPUs.

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Configuration

CD-ROM

※This product was developed as Xtensa Series debugger. It can not be used for software development of the other CPU.

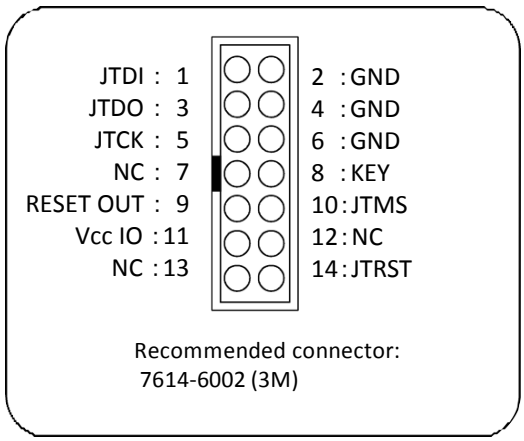
JTAG CABLE types:
SCP8000 : SCP XTENSA

Supported Tool Chains:
WATCHPOINT supports the following compilers and OS:

Compiler:
・Tensilica: C Compiler provided by Tensilica when configuring CPU

Supported OS:
・TOPPERS

Target ICE Connections



Recommended connector:
7614-6002 (3M)

WATCHPOINT Software License

The WATCHPOINT for EJSCT is a licensed software product. One common hardware unit supports other CPU series by acquiring and registering additional software licenses.

* The WATCHPOINT license operates with the registered EJSCT hardware unit only. Once the license is registered with one EJSCT unit, users need to purchase a new WATCHPOINT license in order to use with another EJSCT unit.

Ordering Information

CUSTOMER should PERPARE		Necessary items for Debugger System			
HOST PC	CONNECT WITH PC	JTAG EMULATOR (Hardware)	WATCHPOINT Debugger (software)	JTAG Cable	SUPPORT SERVICE (Software updates)
Windows PC	USB2.0/1.1 CONNECTION	SCD001: EJ-SCT	SCM0800E: WP DBG for EJS Xtensa SCM0801E: WP DBG for EJS Xtensa MC	SCP8000: SCP XTENSA	SSS010: Sophia Support Service

Items in the box surrounded by bold lines are necessary for Systems.
The EJSCT JTAG emulator serves as the hardware key when using software license

System requirements for WATCHPOINT:

OS : Windows Vista/7 (32 bit, 64 bit)
Memory : Minimum memory requirements are amount of memory recommended for each operating system by the operating systems vendor.
Hard Disk : 50MB for installation

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(Ver.140715)

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Please contact us about the prices