Universal Probe

Hardware Users Manual

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Manufacturer	Information	
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Notes

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- 1. Permission from the Japanese government is required when exporting the product and technologies described in this document to which the "Foreign Exchange and Foreign Trade Act" applies or bringing them out of Japan.
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This product has been tested and found to comply with EN 61326, "European Standards -Directive 2004/108/EC - "Electromagnetic compatibility (EMC)" as a measuring instrument.

RoHS

(F

This product complies with the Revised RoHS Directive 2011/65/EU (Directive on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment).



If you have any questions, visit the website of **Sohwa & Sophia Technologies Inc.** and obtain the contact information.

URL > <u>http://www.ss-technologies.co.jp/en/index.html</u>



Operating Precautions

	Failure to observe the following precautions may lead to human death or severe injury.
Do	Avoid supplying voltage out of the range specified in the specifications of this product. Supplying the voltage out of the range may cause damage or fire.
Do	When using the target equipped with the ground terminal, ensure that the ground terminals of the target and peripheral equipment are connected. Failure to do so may cause an equipment failure or electric shock. Avoid connecting the ground terminal to the gas pipe. This causes a fire or explosion.
Don't	Do not transport this product with equipment connected. In particular, hold the plug when removing or inserting the cable. Failure to do so may damage the cable, causing a fire or electric shock.
Don't	Observe the following points when handling the cable. Do not damage, process, forcibly bend, twist, pull, putting any object on or heat the cable, moving the cable close to the heating device, or touch the cable with a wet hand. Failure to observe these precautions may cause a fire or electric shock. If the cable is damaged, stop using it.
Don't	When you hear thunders, do not touch the power plug. This causes an electric shock. If the product seems to be damaged by lightning strike, stop using it.
D on't	Do not let a staple, clip or other metal items enter into the product. This may cause a fire or failure.
Don't	Do not use or leave the product in direct sunlight, near heating devices, in an extremely hot or cold environment, under hard vibrations, in dusty area with a large amount of metal dust or oily dust, or noisy area full of spike noise. Do not give strong impact to the product.
Do not disassemble	Do not disassemble, alter or repair the product. This may cause a fire or electric shock.
No wetting	Do not use the product at a place where there is liquid or at a humid place such as bathroom or in vicinity to glasses. This may cause an electric shock. If liquid enters into this product, immediately turn it off and stop using it.
Caution	Touching the energized product for a long time may cause low-temperature burns. Do not use this product covering with comforter or other cloth.
Pull out the plug.	Immediately turn the power off if unusual smell, noise, smoke or fire is detected or if the product is or may be damaged due to a fall or strong shock. Continuing to use it may lead to a serious accident. Stop using the product.



Abbreviations, Terms and Conventions

This section describes the abbreviations, terms and conventions used in this document.

- About numeric values ... All the numeric values are positive unless otherwise specified. •
- •
- K (capital letter) ... Represents 2^{10} =1024. (Example: 16K=16384)
- k (small letter) •
- ... Represents 1000. (Example: 1kHz=1000Hz)

The annotations and notes used in this document are as shown in Figure 1.

→	Information reference.
(INFO)	Supplementary information.
	Caution. Be sure to read this.

Figure 1



Abbreviations and terms are listed in Table 1.

	Table 1				
Abbreviations and terms	Description				
This product	Universal Probe including accessories.				
This device	Universal Probe itself.				
Serial No.	Stands for the serial number. This means the ID of this device.				
Cofficience Code	Code required to issue the License Code for each software.				
Software Code	Not required for the free edition.				
License Code	Code to add the functions that can be used in this device.				
LA	Stands for Logic Analyzer.				
PG	Stands for Pattern Generator.				
PA	Stands for Protocol Analyzer.				
Host PC	This means the PC used for controlling the Universal Probe.				
Target	Object to be controlled or measured with the Universal Probe.				
Stand along function	Ability to operate without connecting to the host PC.				
Stand-alone function	(The power supply is required.)				
IDE	Stands for Integrated Development Environment.				
(N/A)	Stands for Not Assigned. Indicates that no information is assigned.				
ТСК	Stands for Test Clock. This is a clock for JTAG interface.				
тмс	Stands for Test Mode Select.				
IMS	This controls the state of the connected JTAG TAP controller.				
τοτ	Stands for Test Data In. This is a data input to the JTAG interface.				
	This is an output from this device.				
τρο	Abbreviation of Test Data Out. This is a data output from the JTAG				
100	interface. This is an input to this device.				
TRST(nTRST)	Stands for Test Reset. This is a signal that resets the JTAG TAP controller.				
SRST(nSRST)	Stands for System Reset.				
5131(115131)	This is usually connected to the main reset of a target board.				
RTCK	Stands for Return TCK. This is a clock output from a target board.				
DBGRO	Stands for Debug Request.				
bbong	A target board is stopped from this device for debugging.				
DBGACK	Stands for Debug Acknowledge.				
	This is changed when a target board is stopped by DBGRQ.				
SWD	Stands for Serial Wire Debug.				
SWCLK	Stands for Serial Wire Clock. This is a clock for SWD.				
SWDIO	Stands for Serial Wire Data I/O. This is the data input/output for SWD.				
SWO	Stands for Serial Wire Output. This is the trace data output for SWD.				
	This is an input to this device.				
SWV	Stands for Serial Wire Viewer.				
	This refers to a function to serially output the trace data.				
BSDL file	Stands for Boundary Scan Description Language.				
	The BSDL file is usually obtained from the device manufacturer.				



1. About This Product

1.1. Check of Contents

Contents of this product are listed in Table 2.

If any of the contents is damaged or missing, please inform us through our website.

Table 2				
Appearance	Name	Quantity		
	Universal Probe (Main unit)	1 piece		
and the second sec	USB cable (Accessory)	1 piece		
	Flat cable (Accessory)	1 piece		
	Extension cable (Accessory)	3 pieces		
Water and the second se	Guide	1 piece		
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1.2. Part Names



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		Table 3				
No.	Name	Description				
1	Strap hole	A hole through which a strap is threaded.				
2	POWER LED (Green)	Indicates whether this device is turned on or off. (Light on = $Device ON$ Light off = $Device OEE$)				
		Indicates the operating state of this device.				
			Blinking	Steady ON		
3	STATUS LED (Green)	When the device is NOT in the stand-alone operation.	The LED indicates that the device is communicating with the host PC.	(The LED does not turn ON when this device is not in the stand-alone operation.)		
		When the device is in the stand-alone operation	The LED indicates that the device is operating.	The LED indicates that the device has finished operation normally.		
4	ERROR LED (Red)	Lights up when an en on the function.	ror occurs. Causes of	errors vary depending		
5	USB connector	A connector used for USB cable.	connecting the host	PC with the accessory		
6	I/O connector	A connector used for connecting to a target board.				
\overline{O}	RUN button	A button used for starting a particular operation. The operation varies depending on the function.				
8	Extension connector	Used for connecting to this device externally.	wo or more units of th	is device or controlling		
9	Product label (Serial No. label)	Indicates the serial number of this device.				



 $\langle ! \rangle$

The Serial No. is an important code for identifying each unit. Never peel off, scrape off or other actions to make it illegible. Doing so may void the warranty or make it unable to register additional software.

We cannot reissue the product label.

Do not disassemble this device. The product gets out of warranty if disassembled.



1.3. Main Specifications

Main specifications of this device are listed in Table 4.

	Table 4
Item	Specification
Main unit dimensions	W:119mm x D:69mm x H:14.1mm
Main unit weight	74g
Supply voltage	5.0V±5% USB bus power
Current consumption	Approx. 400mA ^{*1}
USB interface standards	USB 2.0 High-Speed
USB connector	USB Mini-B type
I/O connector	20 pins, 2.54mm pitch
Extension connector	10 pins, 2.54mm pitch
I/O connector input impedance	Approx. 70kΩ
I/O connector output impedance	Approx. 400Ω
Vtref voltage $(V_{IF})^{*2}$	1.2V to 5.0V (±10%)
I/O connector input voltage	$V_{IL} \leq 0.3 \times V_{IF}, V_{IH} \geq 0.7 \times V_{IF}$
I/O connector output voltage ^{*3}	$V_{OL} \leq 0.3 \times V_{IF}, V_{OH} \geq 0.7 \times V_{IF}$
Power output function ^{*4}	1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (±10%) / 40mA (max)
Operating temperature	0 to 55℃
Storage temperature	0 to 60℃

*1: The current consumption may vary depending on the environment of use.

*2: It is impossible to output 5.0V with $\ensuremath{\mathsf{PG}}$

*3: When the terminal is open.

*4: The power output is effective only for particular functions.



1.4. Main Functions

This device provides the following functions when it is combined with various types of software.

Table 5				
Name of software	Function	License		
CMSIS-DAP	This software provides a debug adapter function that can be connected to the environment of Keil MDK-ARM, IAR Embedded WorkBench for ARM, Eclipse (OpenOCD+CMSIS-DAP).	Free		
Boundary-Scan Tool	This tool is used for indicating the I/O status of a device that has the boundary scan function, conducting a wiring test, and others.	Free		
ARM Writer (Size-limited)	This software provides a function of reading and writing data from and to a memory integrated in or connected to ARM CPU. The read/write capacity is limited to 1Kbyte. This software can store the data to be written to the built-in memory or external memory and the writing procedure, and its stand-alone function allows to restore them by pressing the RUN button even without a host PC ^{*2} .	Free		
SPI Writer (Size-limited)	This software provides a function of reading and writing data from and to EEPROM or flash memory through SPI interface. The read/write capacity is limited to 1Kbyte. This software can store data to be written to the ROM and the writing procedure. The stand-alone function allows this device to restore the data and procedure by pressing the RUN button even without a host PC ^{*2} .	Free		
Logic Analyzer/ Protocol Analyzer	This is a logic analyzer for 8ch/100MSa/s sampling. Channels can be extended up to 32 when four units of this device are connected. With the PA function it is possible to analyze and decode particular protocols and trigger the protocols.	Non-free		
Pattern Generator	This is a pattern generator for 8ch/20Mbps output. It can output signals of 0.0V to 3.3V and can also be set to $Hi-Z^{*1}$.	Non-free		
ARM Writer	This software provides a function of reading and writing data from and to a memory integrated in or connected to ARM CPU. This software has the stand-alone function, just like ARM Writer (Size-limited).	Non-free		
SPI Writer	This software provides a function of reading and writing data from and to EEPROM or flash memory through SPI interface. This software has the stand-alone function, just like SPI Writer (Size-limited).	Non-free		
(Debugger made by Sohwa & Sophia Technologies)	This debug adapter function enables connection to our debuggers to be released in the future.	(Non-free)		

*1: The Hi-Z setting is not available depending on the output data rate.

*2: A power source is needed.





To use two or more functions, prepare the required number of License Code for the functions to be used together with this device.

Only one function can work at a time on a unit.

For information on how to obtain various types of software, visit our website.

1.5. Getting a License Code

This device can be used only after you register the serial number and the Software Code and get a License Code.

You cannot use any function, including free software, until you get the license code.

The registration procedure is outlined below. For details, visit our website or refer to the manual of each software product.

- 1) Access the URL shown in the instruction sheet provided with the product, and apply for a License Code.
- Get a License Code.
 You need the License Code to use the software.
 You will get the License Code by email, so you must provide a valid email address.
- 3) Download the software you want to use from our website, and install it to your host PC.
- 4) Connect this device to the host PC and register the license of the software you want to use.

You can register the license after starting the software.

5) Now you are ready to use this device.



2. How to Use

This chapter describes how to use this device.

Figure 3 shows an example of connecting this device to the evaluation board "Collage-MX6Q" equipped with our Freescale i.MX6Q processor.



Figure 3



You need to rewrite the firmware when switching the device between CMSIS-DAP and any other function. For details, refer to "Software Users Manual – Firmware Selector".



2.1. Connecting This Device to the Host PC

To connect this device to the host PC, hold the connector of the accessory USB cable and connect it to this device as shown in Figure 4.

When the USB cable is connected, this device turns on automatically.



Figure 4

2.2. Disconnecting This Device from the Host PC

To disconnect this device from the host PC, hold the connector of the accessory USB cable and disconnect it from this device as shown in Figure 5.

Be sure to stop the software before disconnecting this device from the host PC.



Figure 5

If you disconnect this device during debugging or signal output, this device or the target board may become damaged.

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2.3. Connecting This Device to a Target Board

This section describes how to connect this device to a target board.

Fully insert the connector of the accessory flat cable into this device with the projection on the connector facing down.

You can connect either end of the flat cable to this device.



Figure 6

How to connect this device to a target board for each function and the I/O connector pin-out are described in 2.3.1 and subsequent subsections.

Symbols used in the Direction column of each table have the meanings as shown in Table 6.

Table 6

I : Input

O : Output

OC : Open collector output

--- : Not defined

Notation in the form of "A/B" indicates that the pin has both functions of A and B.



2.3.1. CMSIS-DAP

Connect the accessory flat cable to the ARM 20-pin connector of the target board.

To connect this device to a CoreSight 20-pin connector or a CoreSight 10-pin connector, you need a conversion adapter.

If the connector of the target board has no notch, align Pin 1 of the target board with Pin 1 of the flat cable by referring to Figure 7.



Figure 7

For the latest pin-out of the ARM 20-pin connector, visit the website of ARM and go to "Support" and then "Documentation", and search for "ARM JTAG 20."

The pin functions vary depending on whether the JTAG mode or the SWD mode is active. Refer to Table 7 for the JTAG mode and Table 8 for the SWD mode.





■ JTAG mode

 \rightarrow

Keep (N/A) pins unconnected.

Table 7						
Pin No.	Pin name	Direction	Pin No.	Pin name	Direction	
1	Vtref	Ι	2	(N/A)		
3	nTRST	0	4	GND		
5	TDI	0	6	GND		
7	TMS	0	8	GND		
9	TCK	0	10	GND		
11	RTCK	I	12	GND		
13	TDO	I	14	GND		
15	nSRST	I/OC	16	GND		
17	DBGRQ	0	18	GND		
19	DBGACK	Ι	20	GND		



SWD mode

Table 8					
Pin No.	Pin name	Direction	Pin No.	Pin name	Direction
1	Vtref	Ι	2	(N/A)	
3	(N/A)		4	GND	
5	(N/A)		6	GND	
7	SWDIO	I/O	8	GND	
9	SWCLK	0	10	GND	
11	(N/A)		12	GND	
13	SWO	I	14	GND	
15	nSRST	I/OC	16	GND	
17	(N/A)		18	GND	
19	(N/A)		20	GND	

Keep (N/A) pins unconnected.

To use the CMSIS-DAP function with a user-developed target board, provide the user's circuit with our recommended connector and our recommended pin treatment. We recommend the following four types of connectors: For details of recommended pin treatment, refer to "4.2. Recommended Pin Treatment for Target Side."

- 7620-6002PL and 7620-6002BL [3M] … Straight type
- 7620-5002PL and 7620-5002BL [3M] … Light angle type

Users are responsible for checking whether or not our recommended pin treatment affects their circuits.

Note that Sohwa & Sophia Technologies takes no responsibility for any problem that occurs with a user's circuit due to our recommended pin treatment. If you don't accept this, do not refer to our recommended pin treatment.

Our recommended pin treatment is subject to change without notice.

2.3.2. Boundary-Scan Tool

* 2.3.1. The same connection method as for CMSIS-DAP applies, but this tool supports only the JTAG mode.



2.3.3. Logic Analyzer/Protocol Analyzer

Connect to the signal line to measuring with referring Figure 10 and Figure 11.

Figure 9 shows the pin-out of the I/O connector of this device and the pin-out of the flat cable when it is connected.

It is desirable to connect the GND pins of this device to the target. If the number of connected GND pins is insufficient, measurement errors may occur.



Details of pin-out are shown in Table 9. Keep (N/A) pins unconnected.

Idule 9					
Pin No.	Pin name	Direction	Pin No.	Pin name	Direction
1	(N/A)		2	(N/A)	
3	D0	I	4	GND	
5	D1	Ι	6	GND	
7	D2	Ι	8	GND	
9	D3	I	10	GND	
11	D4	I	12	GND	
13	D5	I	14	GND	
15	D6	Ι	16	GND	
17	D7	Ι	18	GND	
19	(N/A)		20	GND	

Table 9



Loose wires can also be used to connect LA or PG Connect as many GND pins as possible.

1) Direct connection

② Connection via the flat cable









Prepare loose wires by yourself.

Note that some loose wires may degrade the performance of this device.



2.3.4. Pattern Generator

Connect to the signal line for outputting a signal with referring Figure 10 and Figure 11.

Figure 12 shows the pin-out of the I/O connector of this device and the pin-out of the flat cable when it is connected.

It is desirable to connect the GND pins of this device to the target. If the number of connected GND pins is insufficient, output errors may occur.





Details of pin-out are shown in Table 10. Keep (N/A) pins unconnected.

Table 10					
Pin No.	Pin name	Direction	Pin No.	Pin name	Direction
1	(N/A)		2	(N/A)	
3	D0	O/OC	4	GND	
5	D1	O/OC	6	GND	
7	D2	O/OC	8	GND	
9	D3	O/OC	10	GND	
11	D4	O/OC	12	GND	
13	D5	O/OC	14	GND	
15	D6	O/OC	16	GND	
17	D7	O/OC	18	GND	
19	(N/A)		20	GND	

Loose wires can also be used to connect LA or PG Connect as many GND pins as possible. (Refer to the previous page.)

2.3.5. ARM Writer (including the size-limited version)

* 2.3.1. The same connection method as for CMSIS-DAP is applied.



2.3.6. SPI Writer (including the size-limited version)

Connect to the signal line for outputting a signal with referring Figure 10 and Figure 11.

Figure 13 shows the pin-out of the I/O connector of this device and the pin-out of the flat cable when it is connected.

It is desirable to connect the GND pins of this device to the target. If the number of connected GND pins is insufficient, operation errors may occur.





Details of pin-out are shown in Table 11. Keep (N/A) pins unconnected.

Table 11					
Pin No.	Pin name	Direction	Pin No.	Pin name	Direction
1	Vtref	I/O	2	(N/A)	
3	(N/A)		4	GND	
5	MOSI	0	6	GND	
7	(N/A)		8	GND	
9	SCLK	0	10	GND	
11	(N/A)		12	GND	
13	MISO	I	14	GND	
15	nSRST	I/OC	16	GND	
17	SSEL	0	18	GND	
19	(N/A)		20	GND	



2.4. Combining Two or More Units

Up to 4 units of this device can be combined for the LA and PA functions only. Up to 32 channels are available with the combined units.

Operations of two or more units of this device can be synchronized by connecting the accessory extension cables as shown in Figure 14.





3. Specifications of Each Function

3.1. CMSIS-DAP

CMSIS-DAP provides the debugging function with the following IDE connected to this device. This function supports the architectures of "Cortex-A, R and M", but may not support some devices depending on the IDE used.

- MDK-ARM (ARM)
- IAR Embedded WorkBench for ARM (IAR Systems)
- Eclipse (Open source)

 Table 12

 Item
 Specification

 Vtref voltage range*1
 1.2V to 5.0V (±10%)

 TCK/SWCLK frequency
 DC to 15MHz

 Supported I/F
 JTAG, SWD

 SWV
 Not supported

 Hot plugging
 Supported*2

Specifications of the CMSIS-DAP function are listed in Table 12.

*1: This is the voltage supplied by the target board. The I/O voltage of this device follows the supplied Vtref voltage.

*2: This device is hot-pluggable before starting up the IDE debugger. This device is not hot-pluggable during debugging or during starting up the debugger.



To confirm devices supported by CMSIS-DAP, obtain the latest information on each IDE.



For more information about hot plugging, refer to each "IDE Connection Manual" (except Eclipse).



3.2. Boundary-Scan Tool

The Boundary-Scan Tool provides the following functions by using JTAG

- Displays the pin condition of a designated device in a waveform.
- Displays a list of pin conditions of a designated device to allow for switching between input and output at each pin ^{*1} and setting the output value.
- Sets the output value and the expected value and automatically checks the input value and the expected value to check wiring of a printed circuit board.

Figure 15 shows the image of boundary scan.

Figure 15 shows the way to check whether an output pin of Device 1 and an input pin of Device 2 are connected properly.

First, the Boundary-Scan Tool sets a value to the output pin of Device 1. If Device 1 and Device 2 are connected properly, the signal is transmitted to the input pin of Device 2. The Boundary-Scan Tool reads the pin state of Device 2 and compares it with the expected value to check wiring.





Specifications of the Boundary-Scan Tool are shown in Table 13.

 Table 13

 Item
 Specification

 Vtref voltage range*2
 1.2V to 5.0V (±10%)

 TCK frequency
 DC to 15MHz

 Sampling rate
 <10Hz (>100ms)

*1: Input only and output only pins are not switchable.

*2: This is the voltage supplied by the target board. The I/O voltage of this device follows the supplied Vtref voltage.



3.3. Logic Analyzer/Protocol Analyzer

The Logic Analyzer provides a function of recording High and Low of an electric signal and shows it in a waveform. By connecting up to 4 Logic Analyzers, it is possible to increase the number of channels to a maximum of 32.

The Protocol Analyzer provides a function of decoding protocols of mainly serial interfaces and showing them in a form easy to read and analyzing the contents for triggering the protocols. The specifications of these functions are shown in Table 14.

The trigger functions are shown in Table 15.

Item	Specification
Input voltage range	0.0V to 5.0V
Input frequency band	In single-unit operation : DC to 25MHz
Input frequency band	In multiple-unit operation : DC to 2.5MHz
Threshold voltage	Can be selected from 0.6V, 0.75V, 0.9V, 1.25V, 1.66V, 2.5V and 3.0V
Number of channels	8 channels (Can be increased to up to 32 channels by combining 4 units)
Sampling speed	When the internal clock is used : 1kSa/s to 100MSa/s
(in single-unit operation)	When the external clock is used : DC to 25MSa/s
Sampling speed	When the internal clock is used : 1kSa/s to 10MSa/s
(In multiple-unit operation)	When the external clock is used : DC to 10MSa/s
Memory canacity and	50MSa/s to 100MSa/s : High-speed memory 16Kbit/ch = 327us (max)
recording time	200kSa/s to 25MSa/s : Large-capacity memory 100Mbit/ch= 500s (max)
	1kSa/s to 100kSa/s : HDD
Rit ckow	In single-unit operation: < 3ns
Dit Skew	In multiple-unit operation: < 30ns
	Pattern edge trigger, sequential trigger, protocol trigger and external trigger
Trigger functions	AND/OR conditions can be set for these trigger functions. Only AND
	conditions can be set for multiple-unit operation.
Trigger point setting	0% to 100%
Trigger count setting	1 to 100 times
Protocol analysis function	Available (UART, I2C, SPI, CAN 2.0)

Table 14



Pay close attention to the upper limits of the sampling speed and the input frequency band during multiple-unit operation.



	Table 15		
Type of trigger	Specification		
Pattern edge trigger	Leading edge, trailing edge, both edges, High level and Low level		
Sequential trigger ^{*1}	It is possible to create up to 256 patterns of trigger sequence (by selecting High, Low or Don't Care).		
Protocol trigger ^{*1}	 UART: Start, Data, Stop, Parity, ParityError and StopError I2C: Start, Slave Address, Read Packet, Write Packet, ACK, NACK, Data, Repeated Start and Stop SPI: Data CAN: SOF, BaseID, ExtID, RTR, SRR, IDE, R1, R0, DLC, Data, CEC, ACK, EOF, Overload, Error, CRC Error and NACK 		
External trigger	Leading edge and trailing edge		

*1: It is not possible to use the sequential trigger and the protocol trigger at the same time.



3.4. Pattern Generator

The Pattern Generator provides the function of outputting any user-created digital waveform. It can also regenerate the waveform data acquired by the Logic Analyzer. Specifications of the Pattern Generator are shown in Table 16.

	Table 16
Item	Specification
Output voltage (V _{IF})	1.2V, 1.5V, 1.8V, 2.5V, 3.3V
Output voltage range ^{*1}	0.0V $\sim~(V_{IF})V~$ [$V_{OL} \leq 0.3 \times V_{IF}, V_{OH} \geq 0.7 \times V_{IF}$]
Output data rate ^{*2}	≤20Mbps (≥50ns)
Output level ^{*1}	High level, Low level and Hi-Z
Number of channels	8ch
Memory capacity	12Kbit/ch
Bit skew ^{*1}	<6.0ns
Dico timo*1	Typical value: 20ns
Rise time	Worst: 30ns
Hi-Z transition time	Approx. 100ns

*1: When the output is open.

*2: The Hi-Z function can be used when the output data rate is 1Mbps or slower.



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When creating a signal waveform using Hi-Z, it is recommended to connect an external pull-up/pull-down resistor of about $1.5k\Omega$ to this device.

When Hi-Z is set with the PG waveform editor, there is some delay (= Hi-Z transition time) in transition from High/Low to Hi-Z in actual output.

Set waveform	100ns	100ns
Actual output		
	Figure 16	
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3.5. ARM Writer (including the Size-limited version)

This is the function of readings and writing data from and to the flash memory integrated in ARM CPU and an external flash memory or SPI flash memory connected to ARM CPU, by using the JTAG interface. Supported target board configurations are shown in Figure 17.

With the size-limited version, which can be used free of charge, there is no limit on the size of data that can be read, but the size of data that can be written is limited to 1Kbyte.

This function can be operated in stand-alone mode. For the stand-alone operation, refer to "3.7. Stand-alone Operation."



	Table 17	
Item	Specification	
Vtref voltage range ^{*1}	1.2V to 5.0V (±10%)	
TCK frequency	DC to 15MHz	
Maximum writing capacity	8Gbit (max)	

*1: This is the voltage supplied by the target board. The I/O voltage of this device follows the supplied Vtref voltage.



It is impossible to supply power to the target board from this device. When this function works regardless of the presence or absence of Vtref, it supports only 3.3V JTAG interface.



3.6. SPI Writer (including the Size-limited version)

This is the function of reading and writing data from and to EEPROM or a flash memory through the SPI interface.

Supported target board configurations are shown in Figure 18.

With the size-limited version, which can be used free of charge, there is no limit on the size of data that can be read, but the size of data that can be written is limited to 1Kbyte.

This function can be operated in stand-alone mode. For the stand-alone operation, refer to "3.7. Stand-alone Operation."



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Item	Specification
Vtref external supply voltage range ^{*1*3}	1.2V to 5.0V (±10%)
Vtref internal supply voltage range ^{*2*3}	1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (±10%) / 40mA (max)*4
SCK frequency	DC to 15MHz
Maximum writing capacity	8Gbit

*1: Specification when the I/O power is supplied from the target board.

*2: Specification when the I/O power is not supplied from the target board.

*3: Internal and external Vtref voltages are exclusive to each other.

*4: When the target board operates at 40mA or higher, supply power from any other device than this device.



This function provides three choices for the I/O voltage and the power output from the Vtref pin (\rightarrow Refer to Table 19).

The voltage of the internal power source can be selected from the Vtref internal supply voltage range as shown in Table 18.

Table 19				
Mode	I/O voltage of this device	Image of connection		
External power source	External supply voltage	External power source 2.5V signal Target this device When the I/O power of this device is supplied from the target board via Vtref.		
Internal power source (without power output)	Internal supply voltage	2.5VExternal power source2.5V signal2.5V signalTargetthis deviceWhen the target board has a power source, but the I/Opower of this device is not supplied from the target boardvia Vtref. The internal power source generates the voltagesuitable for the I/O voltage of the target board.		
Internal power source (with power output)	Internal supply voltage	Vtref Internal power source Target When the target board has no power source. This device supplies power to the target (and the I/O power) via Vtref.		



3.7. Stand-alone Operation

The stand-alone operation allows this device to store data to be written and the writing procedure and execute the stored process independently, triggered by the RUN button, when this device is powered but not connected to the host PC.

1) Storing data to be written and the writing procedure

Connect this device to the host PC and write data to the target board in the normal procedure. When doing so, this device stores the data to be written and the writing procedure.





2) Disconnect probe from host PC.

Disconnect the probe from the host PC and connect to the target.





3) Connecting the power supply and pressing the RUN button

Supply the power to this device, for example, from a rechargeable battery, confirm that the POWER LED of this device is lighting, and press the RUN button.



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4) Perform writing.

During writing, the STATUS LED blinks.



5) When the writing completes, the LED indicates the result.

When the writing has finished normally, the STATUS LED lights in green and when the writing has finished with an error, the ERROR LED lights in red.





[When finished normally]

[When finished with an error]

Figure 23



4. Appendix

4.1. Extension Connector Pin Assignment

The extension connector is used for linkage operation of two or more units of this device and for communication of trigger information and operation results between this device and external equipment. The extension connector is located at (8) in Figure 2.

The pin-out of the extension connector is shown in Table 20. Keep (N/A) pins unconnected. For the notation in the Direction column, refer to Table 6.

Table 20				
Pin No.	Pin name	Direction	Voltage	Description
1	LINKSYNC2	I/O	3.3V	Clock input/output pin 2 for linkage operation
2	LINKSYNC1	I/O	3.3V	Clock input/output pin 1 for linkage operation
3	LINKTRG2	I/O	3.3V	Trigger input/output pin 2 for linkage operation
4	LINKTRG1	I/O	3.3V	Trigger input/output pin 1 for linkage operation
5	(N/A)			(Not used)
6	ERROR	0	3.3V	The meaning of signal varies depending on the function. (\rightarrow Refer to Table 21.)
7	TRGOUT	0	3.3V	The meaning of signal varies depending on the function. (\rightarrow Refer to Table 21.)
8	TRGIN	Ι	3.3V	The meaning of signal varies depending on the function. (\rightarrow Refer to Table 21.)
9	GND			GND pin
10	VIN		5.0V	External power supply pin. Input voltage should be $5.0V\pm5\%$.



Table 21						
	Pin 6	Pin 7	Pin 8			
	[ERROR]	[TRGOUT]	[IRGIN]			
CMSIS-DAP	No function	No function	No function			
Boundary-Scan Tool	No function	No function	No function			
LA/PA	No function	L = Internal trigger output	L = External trigger input (Only the master is effective during linkage operation.)			
PG	No function	No function	L = Output start trigger			
ARM Writer	L = Indication of termination due to an error	L = Indication of normal end	L = Trigger to start writing			
SPI Writer	L = Indication of termination due to an error	L = Indication of normal end	L = Trigger to start writing			



Operation starts when the trailing edge is detected at pin 8 [TRGIN]. Operation starts when either the leading edge or trailing edge is detected for the external trigger input for LA/PA. (settable)



4.2. Recommended Pin Treatment for Target Side

It is recommended to treat pins for target side connected to this device for the CMSIS-DAP or JTAG interface function as shown in Figure 24.

When the target board has no signals of nSRST (system reset), DBGRQ, DBGACK and RTCK, the pins may be left unconnected.

To determine the pin treatment, visit the website of ARM and go to "Support" and then "Documentation", search for "ARM JTAG 20" and read the description.





Revision History

Ver. No.	Revision date	Content of revision
01	09/26/2014	Initial Release.
02	10/29/2014	Correction of typographical errors.
03	11/17/2014	Correction of typographical errors.



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