

Product Brief

WATCHPOINT Debugger for EJ-SCT ARM / ARM Multi Core





Process transitions window

This software is to be used with the JTAG emulator "EJ-SCT"



■ Compact (70mm × 108mm × 17mm) ■ USB bus-powered when using as a debugger or a writer connecting to PC

Features

Writes to on-board and CPU internal flash memory

- Usable as a stand-alone writer without PC
- Writes data by one-touch PLAY button on the unit
- Outputs signals of script execution start and execution end state by external terminals
- Usable as a device for automatic test and upgrade of trial and mass produced products
- Supports ARM7, ARM9, ARM11 and Cortex series
- ■Supports multiple CPUs in one unit ^{%1 %2}
- ■Supports SWD/SWV ^{※4}
- Supports ARM/Thumb state debug

- Supports semi-hosting function
- Supports Linux Debug
 - AMP/SMP Linux debug ^{*1}
 - Boot loader debug
 - Linux kernel driver debug
 - Linux application debug
 - Graphic display of Process transitions and CPU status
- RTOS Task transitions graphic display
- Docking of windows
- ■Supports ETB as an option
- Supports C/C++ languages

Specifications

	1								
Supported CPU	ARM7 core series (ARM7TDMI, ARM7TDMI-S, ARM710T, ARM720T, ARM740T, etc.)								
	ARM9 core series (ARM9TDMI, ARM9TDMI-S, ARM910T, ARM920T, ARM940T								
	ARM9E, ARM946E, ARM966E, ARM922, ARM925, ARM926, etc.)								
	ARM11 core series (AR	RM1136, ARM117	6, etc.), Cortex core series (A15, A9 MPCore, A8, R4, M0/M3/M4)						
User power	VCC 0.8~5.0V		· · · · ·						
Memory space	Entire space is availabl	le to user							
Interrupts	All interrupts are availa	able to user							
Break	The following condition	ns can be set.							
	- Hardware Breakpoin	nts							
	ARM7/ARM9 core ARM11 core		: Max. 2 points ³⁶³ on instruction execution address, memory access or data : Max. 7 points						
			3 on instruction execution address, 2 on memory access and 2 on others						
	Cortex core (A	(15)	:5 on instruction execution address and 4 on memory access						
	(A)	(8/A9 MPCore	:5 on instruction execution address and 2 on memory access						
	(R	R4)	: 7 on instruction execution address and 8 on memory access						
	(M	/0)	: 4 on instruction execution address						
	(M	/I3/M4)	:5 on instruction execution address						
	- Software Breakpoints : Unlimited software breakpoints can be set for RAM and Flash memory								
Trace	For FTB capability : Optional WATCHPOINT add-on software is available								
SWD/SWV ^{*4}	See the reverse side								
Elash memory	It is possible to downlog	ad a user program	a directly to flash memory on target board by debugger						
download	It is possible to download a user program directly to flash memory on target board by debugger								
※1 This function	is supported only by WATCHPOIN	IT Debugger for EJ-SCT	ARM Multi Core.						

2 Up to 10 CPUs can be debugged simultaneously, but the number may be fewer than 10 depending on the CPU internal structure and PC environment.

3 When one of the following functions is in use as for ARM7/ARM9 core, release one hardware breakpoint.

[Software breakpoint, PASS step, Step out, or COME]

%4 SWD is supported by Cortex-A/R/M series. SWV is supported only by Cortex-M series.

Configuration



■CD-ROM (WATCHPOINT)

 This debugger supports Cortex core, ARM7 core, ARM9 core and ARM 11 core CPUs including their licensees and cannot be used for software development of other CPUs.

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■JTAG CABLE types SCP7500 : SCP 20to20 SCP7200 : SCP CortexMx-PB-HF10-JCB

SCP7300 : SCP CortexMx-PB-HF20-JCB VK0019 : TI-ARM exclusive JTAG cable

Supported Languages :

In order to debug high-level languages by WATCHPOINT, the debug information for user program is needed. The following C compliers and assemblers output the most suitable debug information.

The output debug information may vary depending on the version of the compilers and complier options. Contact us for the operation confirmation.

Maker	Compiler, Assembler
ARM	MDK-ARM, DS-5
IAR	EWARM
GreenHills	GHS
GAIO	XCC-V
GNU	GCC
Metaware	Hiah C/C++/EC++ for ARM

Supported OS :

The OS below may not be supported depending on the version of the language. Also optional software may be required to support the OS. Contact us for more detail.

OS										
µ-T-Kernel/Cortex-M3,M4	μT-REALOS/M3	Keil RTX/Cortex-M3								
UDEOS4/Cortex-M3	µC3/Standard	TOPPERS/JSP								
G-OS	NORTi4	Thread X/Cortex-M3								
Other ITRON OS	Linux	L4 µ-kernel								
Windows CE	VxWorks	Symbian OS								

Target Connections

- 3					JT	AG Header (Connec	tor Pin	ı Assi	ignment(Top	View)				
0.1 inch 2×10 Connector				0	0.05 inch 2×5 Connector				0.05 inch 2×10 Connector						
VTRef NC SWDIO SWCLK NC SWO nSRST DBGRQ DBGACK Recomm VTRef	(nTRST) (TDI) (TMS) (TCK) (RTCK) (TDO)	1 3 5 7 9 11 13 15 17 19 conn	ector: 76	2 4 6 8 10 12 14 16 18 20 620-600	VSupply GND GND GND GND GND GND GND GND GND C2 (3M) Ipply	VTref GND GND KEY GNDDetect Recomme SHF-105-C VTRef : C Option ca * SCP720 connecto	1 3 7 9 01-L-D-* Connect able: SC 0 is requir	onnector * (SAM to targe P7200 ed when h	2 4 8 10 TEC) et pow	SWDIO / TMS SWCLK / TCK SWO / TDO NC/EXTb / TDI NRESET Ver Supply h 10 pin board.	VTref GND GND KEY GNDDetect GND GND GND GND GND GND Kecomme SHF-110-C VTRef : C Option ca * SCP7300 connector	1 3 5 7 9 11 13 15 17 19 01-L- 001-L- 001-L- 001-L- 001-L- 001-L- 001-L- 001-L- 001-L- 001-L- 001-L- 0	d conne D-** (Sect to t SCP7 quired w	2 4 8 10 12 14 15 18 20 ector SAM arge 300 hen h	SWDIO / TMS SWCLK / TCK SWO/EXTE/TRACECTL / TCO NC/EXTE/ TDI nRESET TRACEDATA[0] TRACEDATA[0] TRACEDATA[1] TRACEDATA[2] TRACEDATA[3] T TEC) traceData[3] T ETEC) traceData[3] T T T T C) traceData[3] T T T C) traceData[3]

SWD (Serial Wire Debug) interface is supported.

SWV (Serial Wire Viewer) is supported. It is possible to view the values of variables and event information without break during execution.

About WATCHPOINT Software License

The SSS key is required to use this product. The SSS key is written on the SSS (Sophia Support Service) registration certificate. Multiple types of WATCHPOINT licenses can be assigned (related) to one JTAG emulator.

* Once a WATCHPOINT license is assigned to a JTAG emulator, you will be able to use the WATCHPOINT license only with the related JTAG emulator. When you wish to use with other JTAG emulator you need to purchase another WATCHPOINT software.

Ordering Information

To be prepared	I by customer	Items you need to	Options		
Host PC * 1	Connection to PC	JTAG Emulator Hardware & Software	Support service	JTAG cable (Select at least one cable to fit the target connector)	Software
Windows PC	USB2.0/1.1	SCD001 : EJ-SCT SCM0790E : WP DBG for EJS ARM SCM0791E: WP DBG for EJS ARM MC	SSS010 : Sophia Support Service	SCP7500 : SCP 20to20 SCP7200 : SCP CortexMx-PB-HF10-JCB SCP7300 : SCP CortexMx-PB-HF20-JCB VK0019 : TI-ARM exclusive JTAG cable	U4A401: WP4ARMETB * Required for ETB trace capability

Items in the box surrounded by bold lines are required to build a standard debugging system. The JTAG emulator is served as the hardware key to use the debugger software license

*1 Host PC OS : Windows Vista/7

Minimum memory requirement : The amount of memory recommended for each OS by OS vendor. HDD: At least 500MB of free hard disk space when installing.

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